

ATTIPIC project.

Avionique Très Intégrée pour Petites Plateformes Incluant des COTS



Objectives: Study a generic Avionics architecture (including embedded software) based on COTS as well as a production methodology to be competitive in small satellite platform market. Make a POC on an architecture initiated by the CNES through their Darwin studies and find solutions to cover the identified locks. Mount the solution in matured form for a transfer to the industrialization of the solution



6,5 M
euros



38
months



Thales, CNES, INRIA, SII,
SYRLINKS, STEEI



20
Delivrables

Needs / Locks

- Market for mini-satellite constellations (50 to 250kg)
- Transition from space avionics to the use of Multicore SOC and COTS
- Be competitive compared to new low-cost players, while guaranteeing mission availability close to the state of the art in space.

Locks to solve:

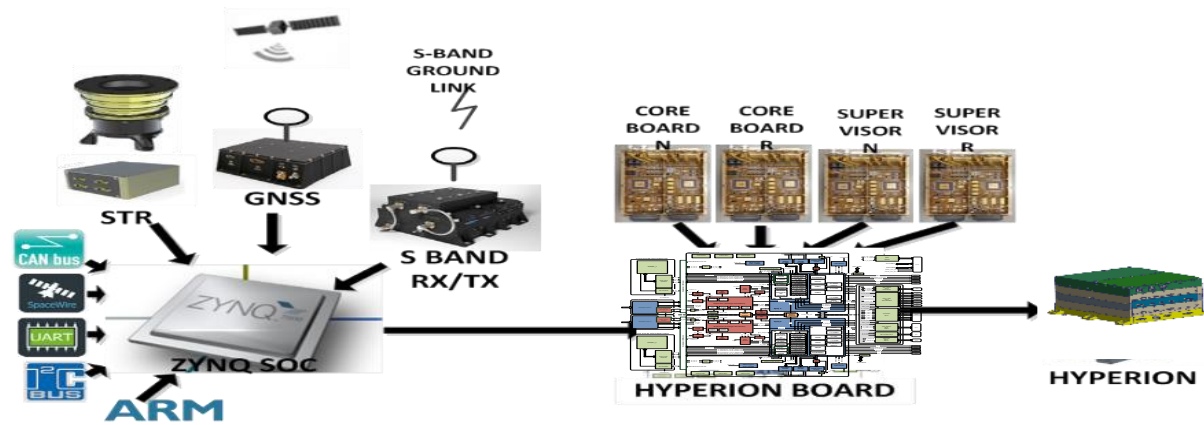
- The use of COTS HW in a space environment,
- the centralization of avionics functions due to the duplication of CPU and memory resources,
- Define a reference architecture supporting different levels of criticality,
- the adaptability of generic cores and production tools to various avionics interfaces,
- Analysis of mitigation mechanisms to obtain a QoS,
- the operational maturity of fault tolerance,
- Predictability in a multi-core setting.

Technical approach

Identification and implementation of the techno necessary to use a multi-core SoC (hypervisor, FPGA chain), identification of services to be provided to facilitate application development (pre-integrated service framework) including mitigation mechanisms. Modelling work with Inria to support the development of an integrated system, with a focus on traffic congestion and system availability issues.

Demonstrate the ability to use these technologies for space through a POC to demonstrate the integration of new technologies and IPs associated with the characteristics of a SOC

Annexes.



Objectives

- to provide support for understanding the hardware architecture of the Zynq processor and especially the interconnects and buses properties and behavior
- to identify the data flow congestion on the computer architecture communication buses including the SoC level (Zynq)
- to estimate the effects of interferences including the use of DMA to achieve massive data/memory transfer

Method and Tools based on MBSE as an early design verification method to predict contentions

- Capella for hardware and software modelling (Physical Architecture of the Arcadia workflow)
- Kitalpha for model refining, components specialization and adding properties for simulation
- Gemoc Studio to define an execution semantic and simulation of the model

Availability-oriented cyber-physical system modelling at microarchitecture level

- Radiation sensitive Computer system's AltaRica model
- SW deployment on HW modelling method

Combine use of MBSE and MBSA tools

- Capella / AltaRica interfacing
- Higher level than AltaRica syntax

Model reusability and availability computing

- Mitigation framework
- Fault Tree generation and stochastic simulation
- Thoughts on Dynamic Fault Trees

Interference model

System availability